WHAT IS CLAIMED IS:

1. A code processing circuit comprising:

a plurality of coders which encode different kinds of data, respectively;

a first buffer which stores the codes outputted from the coders provided corresponding to said plurality of coders;

a second buffer which stores the lengths of the codes outputted from the coders provided corresponding to said plurality of coders;

a first adder which adds the code lengths stored in the second buffer provided corresponding to said plurality of coders;

a second adder which adds all the code lengths added in the first adder; and

an adjustment unit which adjusts an output code by the unit of 1 bit based on the codes stored in the first buffer, the code lengths stored in the second buffer and the code lengths added in the second adder.

2. The code processing circuit according to claim 1, wherein the adjustment unit comprises a code length memory which stores the unit of the output code length; a code length comparator which compares the code lengths added in the second adder with the code lengths stored in the code length memory; an enable signal generator which generates said plurality of different kinds of effective code signals based on the

code lengths stored in the second memory and the comparison result of the code length comparator; and an output code generator which generates output codes by the unit of 1 bit from the codes stored in the first memory and the effective code signals generated by the enable signal generator.

3. The code processing circuit according to claim 1, further comprising a ratio unit which calculates the ratio of the codes outputted from said plurality of kind of data, wherein the adjustment unit cuts off the codes based on the ratio, when the value of the code lengths added in the second adder is larger than the output unit stored in the code length memory.

4. The code processing circuit according to claim 3, wherein the ratio unit has a ratio calculator which calculates the ratio of each code length according to the code lengths added in the first adder and the code lengths added in the second adder.

5. The code processing circuit according to claim 3, wherein the ratio unit has a ratio setting unit which previously sets the ratio of each code length added in the first adder.

6. The code processing circuit according to claim 4, the ratio unit has a ratio setting unit which previously sets the ratio of each code length added in the first adder, and a switching unit which switches and outputs one of the ratio set in the ratio setting

unit and the ratio calculated by the ratio calculator.

7. The code processing circuit according to claim 1, wherein said different kinds of data is red data, green data and blue data.